AMENDMENTS TO THE SPECIFICATION

Please amend the specification as shown below.

Please amend the paragraph beginning on page 16, line 6, with the following amended paragraph:

In digital audio broadcasting, audio information is compressed based on the MPEG audio standard. the compressed MPEG bit stream is coded by convolution coding and time interleaved, then modulated by OFDM modulation and transmitted by a radio wave. Note that to suppress a multipath effect in a transmission path of the radio wave, the broadcasting side provides the OFDM modulated wave with a guard interval for every [symbols] symbol on the time axis, so an OFDM modulated signal comprised of the transmission symbols comprising the guard intervals and effective symbols is actually broadcast.

Please amend the paragraph beginning on page 19, line 15, with the following amended paragraph:

The correlation processing circuit calculates [a] correlation values of data of guard bands with effective symbols in the IQ data and calculates a moving average vector for the lengths of the guard bands and a scalar value thereof. Based on the scalar value of the moving average value of the guard band, a position corresponding to a null-symbol is detected. The resetting of the local time counter of the time base circuit is controlled in accordance with this.

Please amend the paragraph beginning on page 24, line 13, with the following amended paragraph:

The receiving clock generating circuit 130 generates a plurality of divided clock signals that differ in frequencies obtained by dividing the multiplied clock signal CLK by predetermined frequency division ratios, and further, selects one from the plurality of divided clock signals in accordance with the switching control signal S_c from the switching control circuit 220 and outputs the selected one as the receiving clock CK1.

Please amend the paragraph beginning on page 28, line 20, and continuing on page 29, with the following amended paragraph:

The frequency division ratio M of the frequency divider 350 is controlled, for example as shown in Fig. 3, in accordance with the multiplication factor control signals S_M input from the load judgment circuit 210. Since the multiplication factor control signal S_M is controlled in accordance with the processing load of the DSP block, accordingly the multiplication factor of the multiplication circuit 120 is controlled, and the frequency of the multiplied clock signal CLK is controlled. For example, by assuming that the frequency F_0 of the reference clock RCK supplied by the external oscillator 200 is 24.576 MHZ, when the multiplication factor M of the multiplication circuit 120 is controlled at 4 in accordance with the multiplication factor control signal S_M, the frequency of the multiplied clock signal CLK becomes 98.034 MHZ.